REMARKS/ARGUMENTS

Request for Continued Examination:

The applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

Claims 24-26, 29-35 and 38-43 remain in this application. Claims 1-23, 27-28 and 36-37 have been cancelled without prejudice. Though no claim amendment is made in this reply, a claim listing of the claims designated by proper status identifiers is presented for Examiner's convenience.

The Office action of October 16, 2009 misused the prior art (US 2004/0081099, hereafter "Patterson") to reject the pending claims. Applicant respectfully requests for a reconsideration of the current application for at least the reasons set forth herein.

Response to the 35 U.S.C. § 112 rejections:

Claim 43 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. Applicant asserts that the original specification of this application recites: "**[T]he output signal of the controlling device 11 can first feed into a decoding device 12**, and then couple to the detecting device 13 and the multiplexer 16, in order to reduce the number of outputs of the controlling device 11. As shown in Fig. 2B, **the decoding device 12 can be a 3 to 8 decoder (3x8 decoder)**" (*See 3rd paragraph of page 5 of the original specification*). Accordingly, claim 43 is supported by the original specification, and a withdrawal of the 35 U.S.C. § 112 rejections is respectfully requested.

Response to the 35 U.S.C. § 102(e) and 103(a) rejections:

Claims 24-26, 29-33 and 35 are rejected under 35 U.S.C. 102(e) as being anticipated by Patterson (US 2004/0081099). Claims 34 and 38-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patterson in view of Dao (US PAT. 6,407,633). These rejections are respectfully traversed for at least the following reasons.

As for claim 24, it recites:

"[A]n apparatus *(figs. 1, 2A, 2C and 6 for the first embodiment; figs. 3, 4, and 6 for the second embodiment)* for automatically determining a type of an external device, comprising: a jack *(15; 41)* for coupling the external device;

an impedance detecting circuit *(13; 401)*, coupled to the external device through the jack *(15; 41)*, for generating a first analog signal *(DCVOL when transistor Q1 being turned on as shown in fig. 2A, hereafter "DCVOL1"; DC-Sense when connecting switch SW1 with resistor R3 as shown in fig. 4, hereafter "DC-Sense1")* according to an impedance of the external device and a first resistance *(R3 of figs. 2A and 4)*, a second analog signal *(DCVOL when transistor Q2 being turned on, hereafter "DCVOL2" as shown in fig. 2A; DC-Sense when connecting switch SW1 with resistor R4 as shown in fig. 4, hereafter "DC-Sense2")* according to the impedance of the external device and a second resistance *(R4 of figs. 2A and 4)* and a third analog signal *(DCVOL when transistor Q3 being turned on as shown in fig. 2A, hereafter "DCVOL3"; DC-Sense when connecting switch SW1 with resistor R5 as shown in fig. 4, hereafter "DC-Sense3")* according to the impedance of the external device and a third resistance *(R5 of figs. 2A and 4)*, wherein the first, second and third resistances *(R3, R4, R5)* are different;

an analog-to-digital converter *(14; 404)*, coupled to the impedance detecting circuit *(13; 401)*, for converting the first, second and third analog signals *(DCVOL1, DCVOL2, DCVOL3; DC-Sense1, DC-Sense2, DC-Sense3)* to

first, second and third digital values *(referring to the second paragraph of page 9 and fig. 6 which recites that "...the first voltage dividing value also corresponds to 13-15 when the voltage value is converted to a 4-bit digital number...")*, respectively; and

a control circuit *(11; 402)*, coupled to the analog-to-digital converter *(14; 404)*, for determining the type of the external device when the first digital value falls within a first predetermined range *(col. DCVOL1 in Fig. 6)*, the second digital value falls within a second predetermined range *(col. DCVOL2 in Fig. 6)*, the third digital value falls within a third predetermined range *(col. DCVOL3 in Fig. 6)* and all of the first, second and third predetermined ranges together indicate a same recognized condition *(col. Recognized Condition in Fig. 6)* among a plurality of predetermined recognized conditions *(col. Recognized Condition in view of rows Power Speaker1, Power Speaker2, Earphone, Microphone, CD-ROM and Player in Fig. 6)*;

wherein the impedance detecting circuit *(13; 401)* comprises a plurality of resistors *(R3, R4, R5)*, which couples together in parallel, for providing the first, second and third resistance *(R3, R4, R5)* and each of the first, second and third digital values is a multi-bit number *(referring to the second paragraph of page 9 and fig. 6 which recites that "...the first voltage dividing value also corresponds to 13-15 when the voltage value is converted to a 4-bit digital number...")*.

(Note that the related descriptions and element labels in italic are added for understanding)

Accordingly, claim 24 clearly shows that the impedance detecting circuit uses the first, second and third resistances to generate the first, second and third analog signals; the analog-to-digital converter coupled to the impedance detecting circuit generates the first, second and third digital values according to the first, second and third analog signals respectively; and the control circuit determines the type of an external device

with respect to a recognized condition indicated by the first predetermined range containing the first digital value, the second predetermined range containing the second digital value and the third predetermined range containing the third digital value, wherein the first, second and third resistances are different and each of the first, second and third digital values is a multi-bit number.

The Office action of October 16, 2008 misused Patterson to reject claim 24 because:

(1) **the reconfiguration circuit 32e including the resistors R1, R2 and R6 in fig. 9B of Patterson is distinct from the claimed impedance detecting circuit**. According to Patterson, the reconfiguration circuit 32e responds to the identification of a particular load at a particular jack by a load sensing circuit of fig. 9A and reconfigures the circuits associated with the particular jack so that they are properly adapted for the identified load (*See figs. 1, 2, 9A and 9B and paragraphs [0035], [0045], [0059] and [0060] of Patterson*). Consequently, the resistors R1, R2 and R6 of the reconfiguration circuit 32e are used for reconfiguration respectively when analog or digital speakers is detected (*See fig. 9B and paragraphs [0060]-[0061] of Patterson*). Therefore, **the reconfiguration circuit 32e of fig. 9B plays a reconfiguration role for responding to a load identification from a load sensing circuit of fig. 9A rather than plays an impedance detecting role for generating a first, second and third analog signals to identify a particular load.** As a result, the reconfiguration circuit 32e is distinct from the claimed impedance detecting circuit. Besides, **since the resistor R1** (*75 Ohm of fig. 9B*) **is the same as the resistor R2** (*75 Ohm of fig. 9B*), **the resistors R1, R2 and R6 also fail to teach the claimed limitations of "the first, second and third resistances being different"**.

(2) **there is no basis for claiming the ADC of Patterson operating according to the outputs of the reconfiguration circuit 32e to achieve**

the claimed invention. As taught by Patterson, the reconfiguration circuit 32e of fig. 9B is for responding to the load identification of fig. 9A rather than for producing the load identification itself (*See figs. 1, 2, 9A and 9B and paragraphs [0035], [0045], [0059] and [0060] of Patterson*), **and thus the reconfiguration circuit 32e has no reason to provide any output for an ADC such as the ADC 412 of fig. 17 of Patterson**. Even if the reconfiguration circuit 32e provides outputs for an ADC, **since the reconfiguration circuit 32e is NOT properly designed to assist the load identification, its outputs have no help about identifying a particular load**. Therefore, it is not obvious or reasonable to a person of ordinary skill in the art to combine the reconfiguration circuit 32e with an ADC of Patterson to achieve the claimed invention.

(3) **the CPU 12 in fig. 1 of Patterson has nothing to do with the operation of generating the load identification and thereby teaches nothing about the claimed control circuit**. The Office action indicates that the CPU 12 in fig. 1 of Patterson teaches the claimed control circuit. However, Patterson only teaches the load sensing circuit 30 of fig. 1 to send out test signals to loads 24 through connectors 26 and analyzes the responses to determine the identity of each of the loads at each of jacks or connectors 25 (*See fig. 1 and paragraph [0045] of Patterson*), but **Patterson nowhere teaches the CPU 12 producing the load identification in response to a particular load**. Therefore, the CPU 12 dose NOT teach the claimed control circuit.

(4) it is unreasonable to mix up the decision tree embodiment and the simple storage look-up table embodiment of Patterson to anticipate the claimed invention. The Office action took steps of fig. 5 of a decision tree embodiment of Patterson to demonstrate how Patterson reveals the claim limitations of "determining the type of the external device when the first digital value falls within a first predetermined

range, the second digital value falls within a second predetermined range, the third digital value falls within a third predetermined range and all of the first, second and third predetermined ranges together indicate a same recognized condition among a plurality of predetermined recognized conditions", and took circuits and look-up table of figs. 9A, 9B and 10 of a simple storage look-up table embodiment of Patterson to demonstrate how Patterson teaches generating a first, second and third digital values which should be multi-bit numbers to comply with the claimed limitation (*See the Office action of October 16, 2008*). However, Patterson indicates that the decision tree embodiment is distinct from the simple storage look-up table embodiment (*See paragraph [0059] of Patterson*). To a person of ordinary skill in the art, it is obvious that **the decision tree embodiment has no need to use the storage look-up table of fig. 10 to fulfill the load identification and the simple storage look-up table embodiment also has no need to use the decision tree logic of fig. 5 to achieve the load identification**. Under this circumstance, **the Office action does not clarify how these two embodiments are combined, and whether the first, second and third digital values are TIP value of fig. 5 or the outputs JS0, JS1 and JS3 of fig. 10**; meanwhile, the TIP value is different from the outputs JS0, JS1 and JS3 in characteristics and producing source. Assuming that the TIP value is regarded as the claimed digital values, **the TIP value is not generated according to three analog signals respectively associated with three different resistances as recited in the claim** (*See figs. 4-5 and paragraphs [0048]-[0050] of Patterson*). Assuming that the outputs JS0, JS1 and JS3 are regarded as the claimed digital values, **Patterson provides no description about the output JS0 falling within a first predetermined range, the output JS1 falling within a second predetermined range, the output JS3 falling within a third predetermined range and all of the first, second and third**

predetermined ranges together indicating a recognized condition as recited in the claim. Therefore, the Office action does not properly indicate how Patterson teaches the claimed invention while Applicant has shown that it is not obvious to combine the decision tree embodiment and the simple storage look-up table embodiment of Patterson to realize the claimed invention.

(5) **the outputs JS0, JS1 and JS3 in figs. 9A and 10 of Patterson are NOT generated according to three analog signals respectively associated with three different resistances as taught by the claim.** Regarding the way to generate the outputs JS0, JS1 and JS3, Patterson states that: "...two inputs V1 and V2 are delivered to both amplifier 230 and amplifier 232. When V1 is equal to or greater than V2, output JS0 from amplifier 230 is equal to 0, otherwise, JS0 is 1. When V2 is greater than or equal to V1 than JS3, the output of amplifier 232 is 0, else JS3 is one. When V1 equals V2, Js0 is equal to 0 and JS3 is equal to 0...The JS0 and JS3 outputs coupled with the JS1 output effects an identification of a number of different possible devices..." (*See fig. 9A and paragraph [0059] of Patterson*). Accordingly, **the outputs JS0, JS1 and JS3 are generated by comparing the input V1 with the input V2 rather than generated according to three analog signals respectively associated with three different resistances**. Therefore, the outputs JS0, JS1 and JS3 do not match the claimed first, second and third digital values.

For at least the above-mentioned reasons, Applicant respectfully asserts that claim 24 is patentable over Patterson. Since Dao does not compensate for the deficiency of Patterson, Applicant further asserts that claim 24 and the other pending claims are allowable over Patterson in view of Dao for at least the above-mentioned reasons.

Conclusion:

Therefore, all pending claims are submitted to be in condition of allowance. The Examiner is encouraged to telephone the undersigned if there are informalities that can be resolved in a phone conversation, or if the Examiner has any ideas or suggestions for further advancing the prosecution of this case.

Sincerely yours,

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